



**Next Generation
Multi Service Access Node
Universal Line Card
Processor**

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Building Scalable, High-speed Cost-Efficient Multi Service Access Node Line Cards

Telecommunications Equipment Manufactures (TEMs) are facing tough challenges in their triple play concentration and distribution equipment including MSANs. While there are multiple media options to deliver this type of service each media requires a different type of networking component that may handle the required protocols and throughput. This much-talked-about dedicated engineering resources for each media type, which result in huge expenses associated with each media including ADSL, VDSL, Fiber, PON, Transport, Mobile Backhaul and wireless. This type of equipment must now be designed with significantly more bandwidth to support non blocking IPTV, additional protocol handling, traffic management to deliver high QoS, Ethernet and MPLS OAM, Synchronous Ethernet, Content distribution and more stringent multicast performance to support the current IPTV requirements and the future Internet video and appliance including gaming, video and voice conferencing

Another major challenge is being able to offer everything for less.

Increasing bandwidth requirement results with the design of Next Generation Access Node based on 10G dual star architecture that requires dual 10G link towards the backplane. The dollar per port price Telco's will pay for DSL cards has fallen precipitously in recent years, and is not going to change when migrating to ultra high-speed Next Generation Access Platforms. In the face of falling prices, the challenge is to maintain same Access Node platform that can serve low end ADSL cards together with high-end PONs or High-end Mobile Backhaul GbE access line cards..

A third challenge faced by TEMs is the endless need to come up with support for new application, protocol and support the evolving market needs with the need to create a platform that can support new requirements and interfaces without the need to wait for specific silicon implementation, and control the release of the Next Generation Access Node releases.. The equipment vendor will choose to build its solution based on platform that will enable him to differentiate his solution, by enabling fast responds to evolving market needs through the use of Field Programmable Device,

The challenges discussed above translate into a number of requirements for Line Termination Access Processor. In this paper, we begin by examining the Access Processor requirements of MSAN Line Cards, including those needed to address the challenges discussed above. We then move our focus to a brief discussion of the semiconductor industry trends and the ENET architecture features that enable a commercially available FPGA Access Processor. Finally, we discuss characteristics of Ethernity Networks' ENET—the FPGA Access Flow Processor—that make it the right choice for Universal Line Cards

Next Generation Access Aggregation Line Card Processing Requirements

There are a number of features that the ideal Access Processor (AP) must possess to address the challenges discuss above and to meet the demands of next-generation MSAN's.

Throughput: It is critical that the Access Processor have the throughput necessary to enable non blocking performance to all media and ports connected on specific line termination module, and to a newer 10G dual start backplanes to deliver new revenue generating services and to enforce the QoS contracted with all customers. Throughput should be deterministic and not vary based on the type of network traffic internal processing functionality. The Access Processor must allow bandwidth to be flexibly partitioned based on port, service, and direction, all with low line card cost and low power. As the video services portion of the triple play is deployed, the need for throughput and access processor performance in the MSAN line card increases perhaps by an order of magnitude. Not only due to the fact that each port needs to provide more throughput, but the nature of triple play services is to duplicate video stream on the line card for the required ports

that register to specific service. No longer can DSL aggregation bandwidth be so largely oversubscribed. The demands of video streams are too large and too constant to allow the level of over-subscription tolerated in pure data services DSL deployments. The Introducing of GbE access for mobile backhaul, and acceptance of PON FTTx application introduce a minimum of 40Gbps processing needs for MSAN line cards. The throughput of an Access Processor lacking deterministic performance must be measured based on its worst-case performance to assure committed service rates are not impacted when handling “tortuous” protocols.

Flexibility: The ultimate Access Processor will have the exact interface and packet processing capabilities needed for the line card it is designed into. Since it is common for Access Equipment vendors to have a family of line cards for their platform(s), the ideal Access Processor must be available as either a family of devices or as a device with flexible interfaces. If the AP has too many interfaces trying to meet the needs of all, then the line card design will be burdened with additional board area, cost and power needed to support unneeded functionality. Worse, if the AP does not have sufficient interfaces to meet needs, then it either cannot be used or will require additional external devices or logic to compensate for this shortcoming.

An Access Processor should also be capable of supporting the full range of protocols today including PPPoA, IPoA, PPPoEoA, EoA, Tagged Ethernet, SNAP, Q-in-Q, MAC-in-MAC, and MPLS and must have the flexibility to easily handle additional not yet defined protocols in the future

Scalability: While sufficient throughput is needed for high-speed and high port count line cards, a solution that can scale down in price (including external memory), power, and board area is needed for other line cards. System vendors gain product lifecycle efficiencies by using the same technology, components, and suppliers across a wide range of products. AP’s must have the scalability and flexibility to fit in products covering a range of performance and applications. System vendors are looking for a generic interworking and traffic manager solution that can scale for ADSL through VDSL , Ethernet and PONs, which increases OEM scalability and helps reduce carrier CAPEX and improve OPEX .

Low-Power: First and foremost, the Access Processor and its associated memory must remain within the power budget of the system. Some designs operate without external power and total system power is restricted to that available from the twisted pairs. Line cards designed for existing platforms will likely face a firm budget set when the DSLAM platform was first developed. If the AP is significantly below this power budget, the system benefits from higher reliability and potentially greater flexibility in the number and type of cards that can be supported by the platform (the platform’s maximum configuration). Line cards designed for new systems also face stringent power budgets. Now a low power AP gives a number of potential benefits, including: lower system cost, greater system reliability, greater port densities.

Enabling Universal Line Termination Processing

The ENET - the first commercially available Ultra low cost FPGA Access Flow Processor—is enabled by unique architecture that enables the use of low cost FPGA with a combination of low cost DDR2/DDR3 Memory to provide advanced functionality and flexibility and compete with Packet Processor and Network Processors with better functionality, performance and cost. The ENET Family is implemented in FPGA to support up to 40Gbps

Ethernity’s ENET leverages a paradigm shift in ASIC development that enables complex and high-volume designs to cost effectively go to production in FPGA’s. The move to 40 nm process technologies and soon to 28nm and the associated large increase in mask costs and development costs have left only the highest volume applications able to afford the investment required to justify moving a design into the leading edge process. Today FPGAs are implemented in 40nm process technology (28nm in 2011) and offers the logic density, speed, power, and cost advantages associated with this leading edge process technology.

Ethernity's Virtual ASSP solution is enabled by the ENET's highly efficient architecture and by recent advances offering low-cost, high-density FPGA's. The ENET handles classification, framing, packet editing, inverse multiplexing, switching, routing, forwarding, and all traffic management. These functions are handled by a number of pipelined atomic engines. The ENET architecture is very efficient with respect to the amount of logic required for the device: One fourth the number of gates is needed relative to what is found in a typical RISC Access NPU. This gate or logic efficient architecture combined with advanced FPGA technologies has enabled a low-cost FPGA High end 12Gbps Access Processor solution and 40Gbps solution.

Providing reconfigurable modularity to the access processor architecture essentially redefines broadband access line card design and deployment flexibility, scalability and cost savings. The Access Flow Processor provides multiple line interface types and reprogrammable interworking options on a single, modular architecture. Interchangeable line interface units offer a cost effective way to add service interface types and customize line cards - precisely to the port count and packet processing line card demands. Why not get exactly the line interface you need, per port, instead of having to build separate line cards? Reconfigurable, build-as-you-need-it deployments can substantially reduce capital costs. The ability to add incremental bandwidth accommodates unpredictable growth and changing traffic patterns, and eliminates costly unused ports.

In fixed line card architecture, the need for different port counts & service types forces the TEM to develop multiple line card designs based on different packet processors which increases initial costs and creates bandwidth specific solutions. Inflexibility also increases total cost of ownership because it multiplies the number of development teams and limits cross-platform scalability.

In contrast, the ability to address multiple service types and port counts with a single reconfigurable access packet processor architecture substantially lowers overall system cost and provides a scalable bandwidth independent solution. Flexible line interface options and protocol interworking functions can enhance network performance, evolution and multiple-service convergence while reducing operational complexity and expenses. Going forward, the Access Flow Processor unique capabilities enables flexible access line card design and scalability to simplify future growth.

The table below depict the development cost associated with design of multiple line card based on fixed access line card architecture. This assume a non blocking solution that operate at line speed for all ports, hence each solution is based on a different Network / packet processor

	8-16 port DSL IP DSLAM	48 – 96 ports ADSL IP DSLAM	24-48 ports VDSL	24x GbE ports	4-8 ports of PONs	Total Dev Engineers
Software Engineers	4	4	4	4	6	22
Board engineers	3	4	4	1	4	15
Component solution	Low end processor	3Gbps Network processor	6 Gbps Network processor	40Gbps Network processor	40Gbps Network processor	

Table 1 : Development resource for multiple line cards based on fixed architecture

Comparing the above table we can see easily that using universal line termination processor with reconfigurable interfaces can reduce dramatically the overall development cost

	48 – 96 ports	24-48 ports	24 x GbE	8-16 ports	Total Dev

	ADSL	VDSL	Ports	of PONs	Engineers
Software Engineers	Same SW platform	Same SW platform	Same SW platform	Same SW platform	4
Board engineers	1	1	1	1	4
Component solution	ENET3200x	ENET3500x*	ENET4800x	ENET4800x	

Table 2 : Development resource for multiple line cards based Universal line termination architecture

* ENET3800x will be used for 48 VDSL card with 10Gbps backplane.

Further to this 70% cost reduction in development cost it is clear that OPEX and CAPEX will be reduced in the same amount due to the fact the Telecom Equipment Manufacture will use a single manufacturing and procurement platform for all line termination modules.

ENET FPGA Access Flow Processor Addresses TEM Line Card Requirements

Ethernity Networks ENET Access Flow Processor offers up to 40Gbps deterministic performance, low power, and the capability to handle today’s network traffic and to adapt to tomorrow’s new network protocols and traffic management needs. The ENET is based on several atomic engines providing intuitive programming model to support new protocols, flexible classification and forwarding through the programmability of 32 search table that can search up to 128,000 entries, programmable packet editing and advanced traffic management. Another characteristic of the ENET setting it apart from standard network processors and offering important advantages in access equipment is its FPGA implementation. By offering the ENET Access Flow Processor solution in an FPGA, we offer the access equipment designer a number of advantages associated with FPGA design including: customization of interfaces, ability to upgrade in the field, ability to incorporate other board logic, and rapid development and prototyping.

Performance: Ethernity Networks’ ENET architecture consists of a staged pipeline. The tasks of Parsing, Classification, Forwarding, Traffic Management, SARing, Policing, and Packet Editing are each handled by one or more engines in the pipeline. The data pipeline width is 64/128/256 bits and the engine runs at 100/150/250 MHz. Handling the worst case packet size of 64 bytes, this result in a throughput of 12.5/18/32 MPPS or 10/20/40Gbps.

The ENET’s 40 Gbps network traffic performance is well beyond the capabilities of most Network processors available for Access applications. Network processors that are capable of this throughput are too expensive and consume too much power to be acceptable for typical MSAN line card deployments.

Flexibility: Implementing the Access Processor in an FPGA has many advantages. Key among these advantages is flexibility, which is achieved on several levels. Through the devices many configuration registers and tables, the ENET can be pre-configured or altered on the fly to handle in a very intuitive programming model based on simple API an incredibly large range of network traffic types and traffic management/QOS requirements. The Ethernity FPGA solution offers the flexibility to customize interfaces. GMII, SGMII, XAUI, MII, Utopia, SPI, POS, and unique customer defined interfaces can be combined to suit the needs of the application. With the ENET FPGA solution, the designer is not limited by the interfaces offered by an ASSP vendor. The

Ethernity FPGA solution offers the flexibility to upgrade a product in the field. While products are often deployed with no definitive plans to upgrade or alter installed units, the option of being able to alter the hardware in the FPGA offers important insurance against unforeseen events. This capability is important to many carriers who prefer to future proof their systems with the option of the field upgrade.

Scalability:

The ENET Family can scale from 2 Gbps to 40Gbps. This is accomplished through the selection of the FPGA type and the number of external memory interfaces.

In Table 3 below, we see examples of DSLAM line cards supported by the several ENET3000 versions available.

Line Card type	Product	Interfaces		Simplex Bandwidth		DDR Memory
		Backplane	User	BPS	PPS	
24 x GbE + 2 x XAUI	ENET4800x	2 x XAUI	24 x SGMII	40G	32M	12
8 x GPON + 2 x XAUI	ENET4800x	2 x XAUI	8 x GPON	40G	32M	12
48-ports VDSL2	ENET3800x	2x /XAUI	4 x UT2/PL2	12G	18M	6
48-ports VDSL2	ENET3500x	2 x QXAUI / 4 xSGMII	4x UT2/PL2	6G	12.5M	3
72-port ADSL2+	ENET3200x	2xSGMII	2x UT2/PL2	2.5G	5M	2

Table 3: Example Line Card Configurations

Low-Cost & Low Power: Ethernity delivers its 2 and 12 Gbps solutions in low cost FPGAs and its 40 Gbps solution in more expensive FPGAs. Access Packet processors developed on state-of-the-art 40-nm FPGAs (soon 28nm) have several time-to-market and cost-saving benefits, including design automation, flexibility, and reduced development risk. Ethernity Networks has taken advantage of these benefits to accelerate Access Processor development in the dynamic MSAN market and adapt to standards which are constantly evolving.

Ethernity Networks' ENET family supports line cards for Multi-Service Access Node including 96-port dual latency non-blocking ADSL2+, non-blocking 48-port 100/100 VDSL2, Multi-port Fast Ethernet, Gigabit Ethernet, and Fiber-to-the-Home (FTTH).

A secondary, but very important, benefit of the ENET's cost-efficient architecture is low power consumption. To process a given amount of network traffic, the ENET's optimized architecture uses much less logic and less switching relative to a RISC processor (even when the processor's instruction set is tailored for networking applications). The ENET requires well under 4 Watts while handling 12 Gbps of network traffic.

And finally , Ethernity Virtual ASSP solution offers the capability to add your own logic to the FPGA in order to incorporate miscellaneous board functions into the FPGA. We have observed that many access cards designed with RISC NPU's also required FPGA's to implement features not supported by the NPU (such as framing or channel bonding) and to implement miscellaneous board logic. Ethernity's Access Flow Processor is an access card's only FPGA. Unused logic on

the ENET is available to the user to implement various board logic such as GPIO, timer, or other customer specific functions.

Conclusion

We began with a review of the requirements of Access Processors for MSAN line cards. Next, we saw how combining Ethernity Networks efficient ENET architecture with FPGA's created a family of products tailored to the needs of Telecom Aggregation and interworking platforms. Ethernity's ENET Access Flow Processors have the best combination of performance, feature set, flexibility, and price available.