ENET-D Product Overview

Ethernet Controller DMA Engine FPGA IP Core

Ethernity Networks introduces ENET-D, an FPGA Ethernet Controller DMA engine IP Core specifically built for efficiently processing millions of flows and offering performance acceleration for networking and security appliances.

ENET-D is Ethernity's implementation of an Ethernet adapter and DMA engine for PCIe, eliminating the need for a proprietary ASIC serving as the Ethernet controller, to allow complete disaggregation of the Ethernet controller on an FPGA SmartNIC by fitting into different FPGAs and scaling in the amount of queues, physical functions, virtual functions, and other contexts.

The ENET-D can be combined with Ethernity's ENET Flow Processor and run on Ethernity's cost-optimized and affordable ACE-NIC100 FPGA SmartNIC to deliver Router-on-a-NIC with integrated Ethernet controller, capable of connecting to multiple virtual machines, containers, or virtual networking functions. ENET-D provides both Linux kernel drivers and DPDK drivers.

Product Highlights

- Supports 512 RX and 512 TX DMA queues, extensible upon request
- Supports SR-IOV with 4 Physical Functions (PF) and 252 Virtual Functions (VF)
- 256 Virtual Machines, extensible upon request
- Supports PCIe Gen2, Gen3, and Gen4
- Supports 256-bit and 512-bit data path
- Dynamically reconfigurable per queue of DMA channel Source and Destination, buffer size, mode of operation, interrupt mode etc.
- Scatter-Gather descriptor-based DMA with dynamic DMA control per descriptor
- Circular descriptor buffers ring for packet transmission and reception
- Internal DMA channel Context Memory

ENET-D Provides Value

- Accelerates performance for networking and security appliances
- Complete Router-on-NIC when combined with ENET Flow Processor
- Saves long-term operating costs by disaggregating Ethernet controller from ASIC-based hardware
- Integrates with various FPGAs

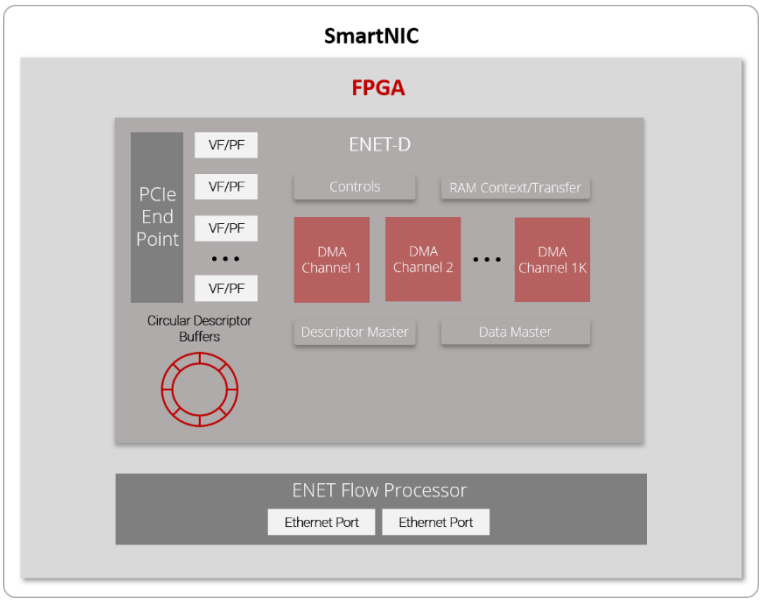

Figure 1: The ENET-D, when combined with the ENET Flow Processor, offers a complete Router-on-a-NIC with integrated Ethernet controller, or it can be used with an Ethernet MAC to serve as a DMA controller

Features

General
- Supports simultaneous RX and TX implementation in ENET-D blocks
- Supports parallel operation of data handler, descriptor fetch, descriptor write back, and timer coalescing/throttling mechanisms
- Single clock domain design
- Supports on-the-fly removal (invalidate) and addition (enable) of queues
- Supports packet/timeout coalescing mechanism and interrupt throttling mechanism
- Each queue is fully configurable and fully independent

Drivers
- Open source drivers provided
- Both kernel drivers and DPDK drivers
- Supports both polling mode and interrupt mode

Descriptor
- Supports descriptor-based mechanism with 16/32-byte descriptor format on RX side and 16/32-byte descriptors on TX side (4 descriptor types)
- Supports packet split to multiple buffers
  - 8 data buffers for RX
  - 8 data buffers for TX
- Supports header split mechanism to split a packet into header buffer and data buffer
  - Also supports zero data case (only header)
- Supports block fetch (read) and write back of descriptors
  - 128 descriptors for read/write per block
- Contains internal descriptor memory for pre-fetched descriptors (per queue for both RX and TX queues)
  - Memory size is configurable

Interfaces
- I/F to Ethernet MAC
  - Supports status per queue – byte and packet per RX queue, fetch and write back status
  - Supports separate RX and TX data interfaces
- I/F to PCIe core
  - Includes PCIe wrapper block that can be adapted to various PCIe cores

Debug
- Mechanism that allows read and write of internal descriptor memory
- Debug register that reflects the ENET-D state machines and interface control signals
- Contains error register that reflects errors that occurs in the ENET-D unit

Interrupt and Error Handling
- Supports 2048 MSI-X vectors
- Supports interrupt coalescing mechanism per ENET-D queue
  - Interrupt once per N packets
  - Interrupt after M time from last processed packet
- Supports interrupt throttling mechanism
  - Guarantees minimum time L between two consecutive interrupts
- Supports interrupt signaling toward the host for lack of descriptor using low threshold mechanism
- Supports error interrupt

Arbitration
- Fetch arbiter for both TX and RX DMA
- Write back arbiter for both TX and RX DMA
- Data hander arbiter for TX DMA
- Data handler arbiter for RX DMA
- Write arbiter toward the PCIe
- Read arbiter from the PCIe
- Arbitration contains the following mechanisms:
  - Round robin
  - Strict priority

Statistics
- Per queue statistical counters for packet and bytes for:
  - Descriptor fetch
  - Descriptor write back
  - RX data received (bytes and packet)
  - RX discard data (bytes and packets)
  - TX data transmitted (bytes and packets)

ENET-D Enables Power Savings

- The ENET-D Ethernet controller firmware consumes much less logic than its competitors
- This enables it to fit into a small FPGA and to consume 2X-3X less power than similar Ethernet controllers on the market